Please amend the subject application as follows:

IN THE CLAIMS:

Please cancel claim 20 without prejudice.

1. (previously presented) A memory device comprising:

a first memory array having a plurality of first memory cells, wherein each one of the plurality of first memory cells is arranged at an intersection of at least one of a plurality of wordlines, at least one of a plurality of bitlines, and at least one of a plurality of digit lines;

a second memory array having a plurality of second memory cells, wherein each one of the plurality of second memory cells is arranged at an intersection of at least one of the plurality of wordlines, at least one of a first reference bitline and a second reference bitline of the plurality of bitlines, and at least one of the plurality of digit lines;

a current providing unit for providing a second current to the first and second reference bitlines in response to a reference voltage; and

a sense amplifier for comparing a first current flowing through one of the plurality of bitlines with the second current, wherein each one of the plurality of second memory cells set to a first logic state is coupled to the first reference bitline and each one of the plurality of second memory cells set to a second logic state is coupled to the second reference bitline.

2. (previously presented) The memory device of claim 1, wherein the current providing unit comprises:

a first current mirror coupled to the first reference bitline, wherein a current from the first reference bitline flows through the first current mirror in response to the reference voltage;

a second current mirror coupled to the second reference bitline, wherein a current from the second reference bitline flows through the second current mirror in response to the reference voltage; and

a third current mirror for providing half of the sum of the current from the first bitline and the current from the second reference bitline to the sense amplifier.

3. (canceled)

4. (previously presented) The memory device of claim 1, further comprising a circuit for clamping a voltage of a first data line through which the first current is transmitted, and a voltage of a second data line through which the second current is transmitted, to the reference voltage when one of the plurality of wordlines of one of the plurality of first memory cells is enabled.

5. (original) The memory device of claim 1, wherein the first memory cells and the second memory cells are magnetic.

6. (original) The memory device of claim 1, wherein the first current is a

target current.

7. (original) The memory device of claim 1, wherein the second current is defined by the expression (i(H)+i(L))/2.

8. (original) The memory device of claim 1, wherein the second current is a reference current.

9. (original) The memory device of claim 1, wherein the first current is compared to the second current to determine a logic state of a predetermined one of the plurality of first memory cells.

10. (previously presented) A memory device comprising:

a plurality of first bitlines and a plurality of second bitlines;

a first memory array having a plurality of first memory cells;

a second memory array having a plurality of second memory cells;

a current providing unit for providing a second current to one of the plurality of second bitlines in response to a reference voltage;

a sense amplifier for comparing a first current flowing through one of the plurality of first bitlines with the second current; and

a circuit for clamping a voltage of a line through which the first current is transmitted, and a voltage of a line through which the second current is transmitted, to the reference voltage.

11. (original) The memory device of claim 10, wherein the current providing unit comprises:

a first current mirror coupled to a first one of the plurality of second bitlines;

a second current mirror coupled to a second one of the plurality of second bitlines; and

a third current mirror for providing half of the sum of a current from the first current mirror and a current from the second current mirror to the sense amplifier.

12. (original) The memory device of claim 10, wherein each one of the plurality of second memory cells set to a first logic state is coupled to a first one of the plurality of second bitlines and each one of the plurality of second memory cells set to a second logic state is coupled to a second one of the plurality of second bitlines.

13. (canceled)

14. (original) The memory device of claim 10, wherein the first memory cells and the second memory cells are magnetic.

15. (original) The memory device of claim 10, wherein the first current is a target current.

16. (original) The memory device of claim 10, wherein the second current is defined by the expression (i(H)+i(L))/2.

17. (original) The memory device of claim 10, wherein the second current is a reference current.

18. (previously presented) The memory device of claim 10, wherein the first current is compared to the second current to determine a logic state of a predetermined one of the plurality of first memory cells.

19. (previously presented) A memory device comprising:

a plurality of bitlines intersecting with a plurality of wordlines and a plurality of digit lines to form a plurality of memory cells;

a sense amplifier; and

a current providing unit electrically coupled to the sense amplifier for providing a reference current to the sense amplifier, wherein:

the sense amplifier compares a current flowing through a first one of the plurality of bitlines with the reference current; and

the current providing unit comprises:

a first current mirror coupled to a second one of the plurality of bitlines;

a second current mirror coupled to a third one of the plurality of bitlines; and

a third current mirror for providing the reference current equal to half of the sum of a current from the first current mirror and a current from the second current mirror to the sense amplifier.

20. (canceled)

21. (previously presented) A memory device comprising:

a first memory array having a plurality of memory cells connected with one of a plurality of wordlines, wherein each one of the memory cells stores either one of a first logic state and a second logic state;

a second memory array having a plurality of first reference memory cells set to the first logic state and a plurality of second reference memory cells set to the second logic state, wherein the first and second reference memory cells are connected with one of the plurality of wordlines;

a circuit for clamping a voltage of a first data line through which a first current is transmitted to a selected memory cell, and a voltage of a second data line through which a second current is transmitted to the first and second reference memory cells, to a reference voltage when one of the plurality of wordlines of one of the plurality of memory cells is enabled;

a reference current providing unit for providing a first reference current and a second reference current to the first reference memory cells and the second reference memory cells respectively, in response to the reference voltage, wherein an average of the first and second reference currents is the same as the second

current; and

a sense amplifier for sensing the logic state of a selected memory cell by comparing the first current with the second current.